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(54) Digital noise generator

(57) A digital noise generator is provided for producing white noise during a period when a digital telephone speech signal is absent. The digital noise generator comprises a pseudo-random bit sequence generator (43), an amplitude control circuit (51) and a PCM code-word-generating shift register (52), wherein a pseudo-random bit sequence is generated by the pseudo-random bit sequence generator (43), an amplitude code-word is generated by the amplitude control circuit (51), and a pseudo-random noise signal is generated and outputted by the PCM code-word-generating shift register (52) having regard to the pseudo-random bit sequence and the amplitude code-word.

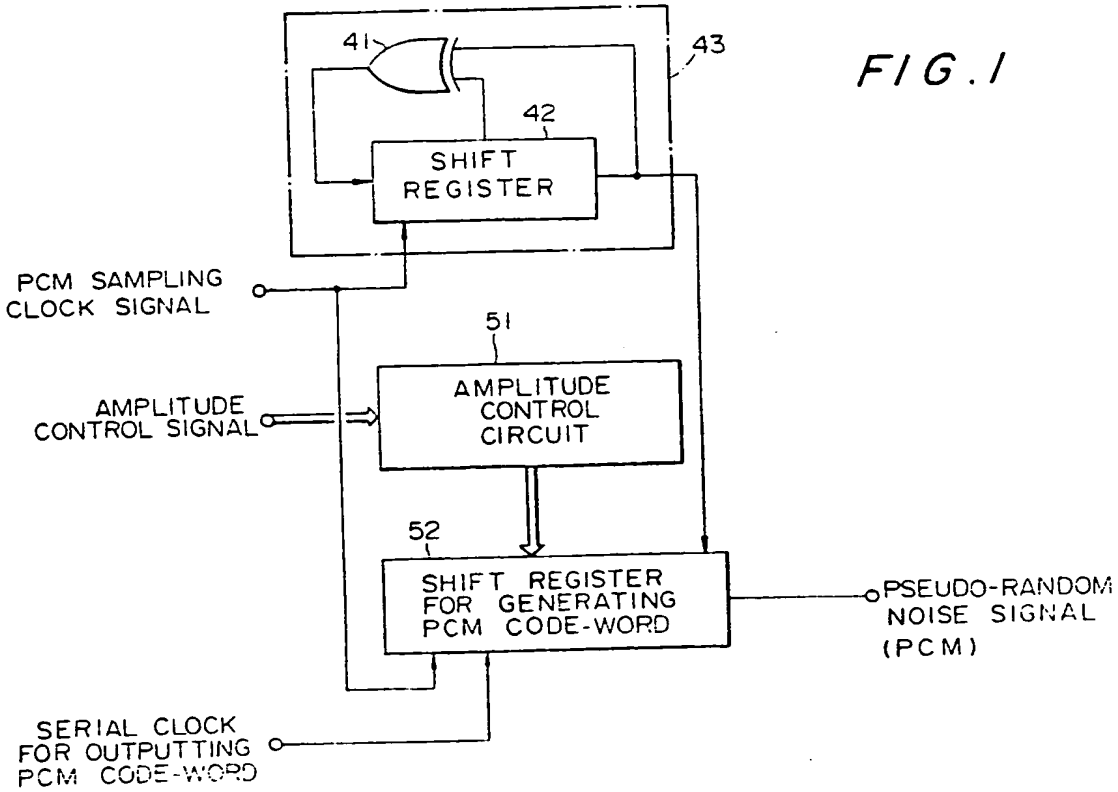

FIG. 1

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FIG. 1

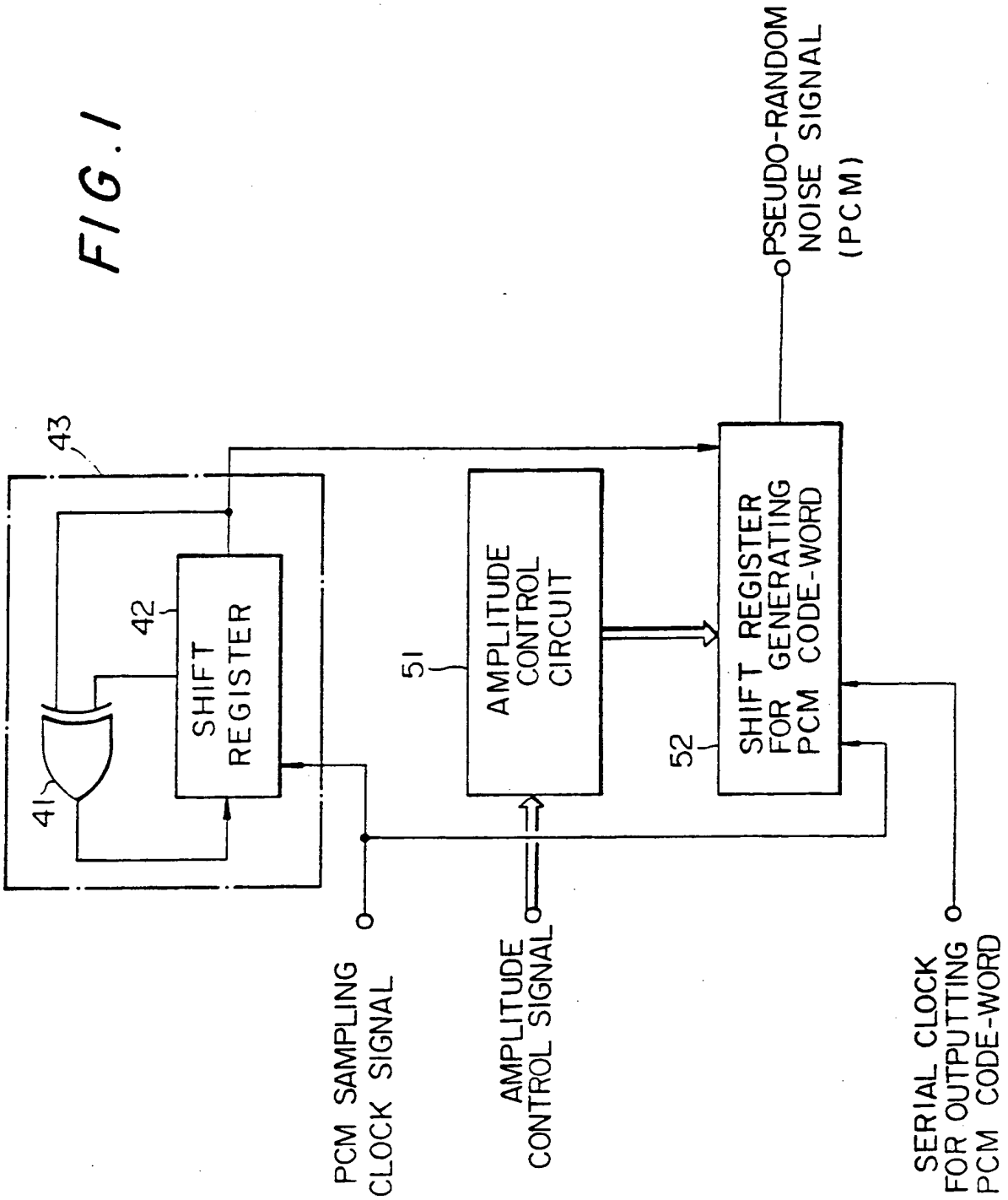

43
42
SHIFT REGISTER
41
51
AMPLITUDE CONTROL CIRCUIT
52
SHIFT REGISTER FOR GENERATING PCM CODE-WORD
PSEUDO-RANDOM NOISE SIGNAL (PCM)
PCM SAMPLING CLOCK SIGNAL
AMPLITUDE CONTROL SIGNAL
SERIAL CLOCK FOR OUTPUTTING PCM CODE-WORD

FIG. 2

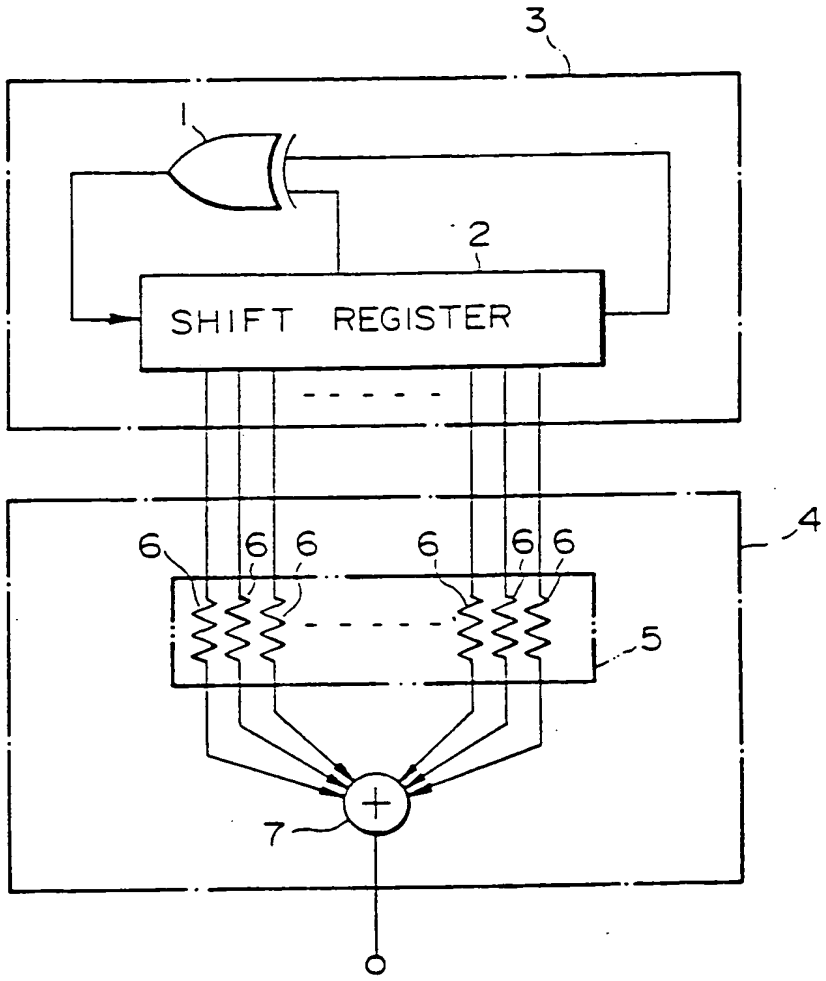

3
1
2
SHIFT REGISTER
4
6
6
6
6
6
6
5
7
PSEUDO-RANDOM
NOISE SIGNAL (PAM)

FIG. 3

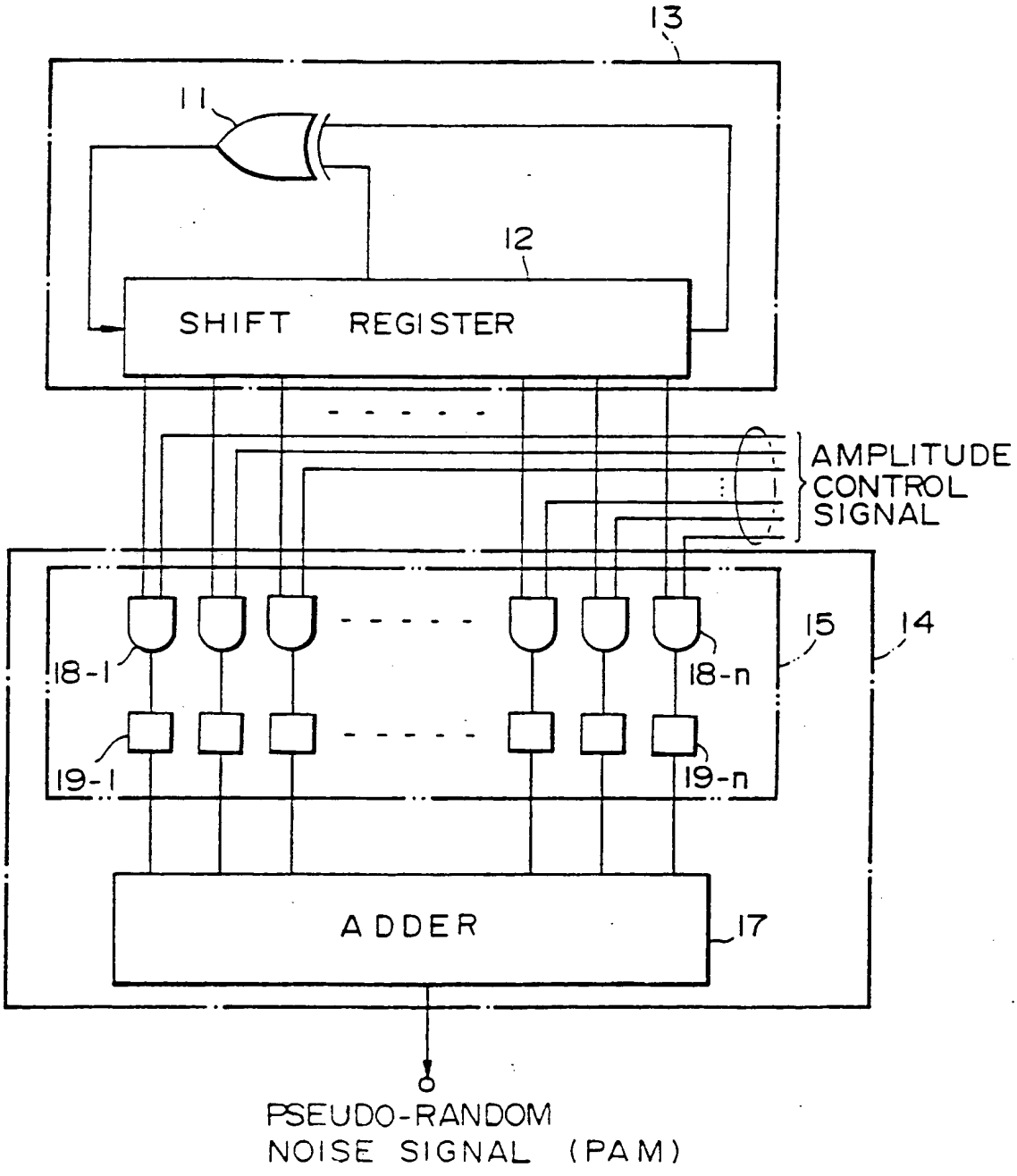

13
11
12
SHIFT REGISTER
AMPLITUDE CONTROL SIGNAL
18-1
18-n
19-1
19-n
15
14
ADDER
17
PSEUDO-RANDOM NOISE SIGNAL (PAM)

FIG. 4

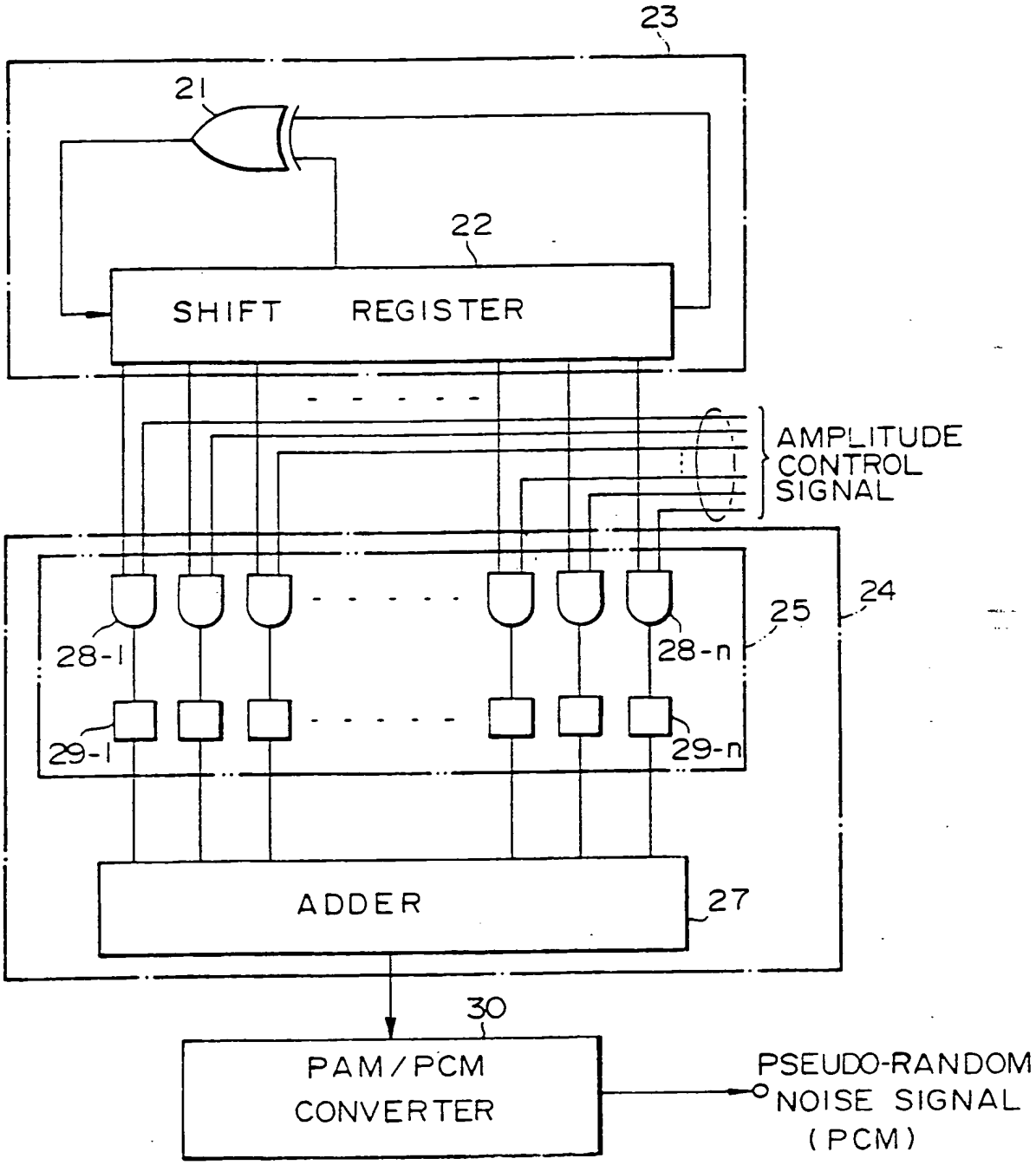
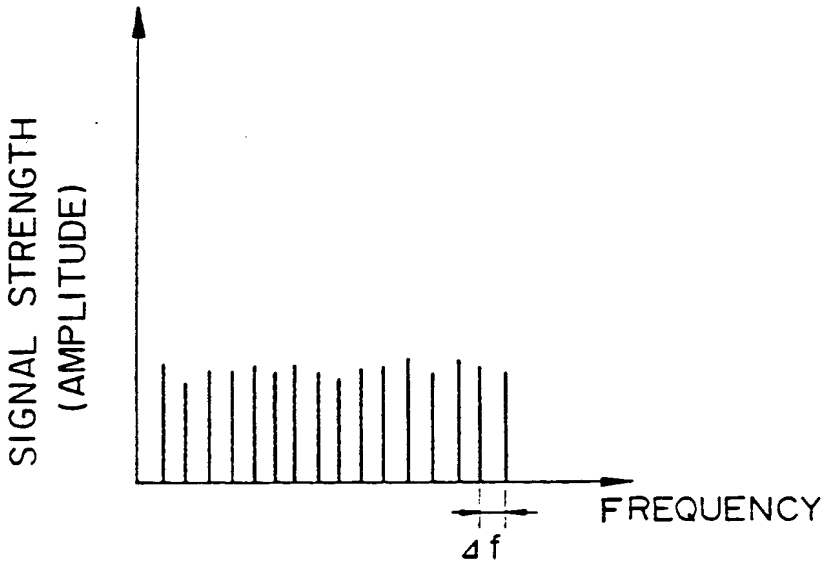

23
21
22
SHIFT REGISTER
AMPLITUDE CONTROL SIGNAL
24
25
28-1
28-n
29-1
29-n
ADDER
27
30
PAM/PCM CONVERTER
PSEUDO-RANDOM NOISE SIGNAL (PCM)

FIG. 5



DIGITAL NOISE GENERATOR

DESCRIPTION

The present invention relates to a digital noise generator for generating pseudo-random noise.

Such a digital noise generator is used to alleviate a listener's discomfort which may occur during so-called inactivity periods when signal transmission does not occur from the speaker side. Specifically, the digital noise generator is employed in digital speech interpolation (DSI) equipment, in which only signals with voice activity are transmitted with digitised telephone speech signals, and digital circuit multiplication equipment (DCME) which comprises DSI equipment in combination with a low-bit-rate speech coding technique and voice packet transmission equipment.

Conventionally, various digital noise generators for generating pseudo-random voice are known.

Fig. 2 illustrates one example of a conventional digital noise generator. This configuration is

disclosed in Japanese Utility Model Publication No. 12446/1989.

This digital noise generator has a pseudo-random bit sequence generator 3 which is composed of an exclusive-OR circuit 1 and an n-bit shift register 2.

Furthermore, this digital noise generator has a pulse amplitude modulation circuit (hereinafter referred to as the PAM circuit) 4. The PAM circuit 4 includes both a weighting circuit 5 including a plurality of weighting resistors 6 and an adder 7 for adding outputs of the weighting circuit 5 together.

A description will now be given of the operation of this digital noise generator.

The exclusive-OR circuit 1 fetches an output and intermediate output of the shift register 2, performs an exclusive-OR operation with respect to these outputs, and feeds back the computed result to the shift register 2. Here, by the intermediate output of the shift register 2 is meant a signal representing the value of a predetermined bit of the n-bit shift register 2.

As a result of the above-described configuration, the value of the bits of the shift register 2 becomes one which is generally called a pseudo-random bit sequence.

Furthermore, since each bit of the shift register 2 is connected to one end of each weighting resistor 6, a signal

obtained by adding the outputs of the weighting circuit 5 by means of the adder 7 becomes a signal representing a value in which the values of the bits of the shift register 2 are weighted and added together, i.e., a pulse amplitude-modulated signal.

The signal thus obtained is called the pseudo-random noise signal. This pseudo-random noise signal is used as white noise in the aforementioned DSI equipment and other similar equipments. In such an application, it is necessary to set the number n of the bits of the shift register 2 to a sufficiently large magnitude.

Fig. 3 illustrates a second example of the circuit configuration of the digital noise generator in accordance with the prior art.

In this circuit configuration, an improvement is made on the configuration of the weighting circuit 5 in the circuit configuration shown in Fig. 2.

In other words, a weighting circuit 15 in Fig. 3 includes an n-number of AND circuits 18 and an n-number of scale factor circuits 19 that are both connected to output terminals of the AND circuits 18.

The bit data of the shift register 12 are respectively inputted to the input terminals of the AND circuits 18, and an amplitude control signal is also inputted thereto from an external circuit.

The amplitude control signal is used to select which bit of the shift register 12 is to be added by an adder 17.

That is, each of the AND circuits 18 outputs the bit data of the shift register 12 to a corresponding one of the scale factor circuits 19 in response to the amplitude control signal. Each of the scale factor circuits 19 weights the data supplied from the corresponding AND circuit 18, and outputs the result to the adder 17. The pseudo-random noise signal is outputted from the adder 17 in the same way as the prior art shown in Fig. 2.

Accordingly, in this prior art it is possible to control the amplitude of the pseudo-random noise signal by adjusting the number of bits to be added by means of the amplitude control signal.

Fig. 4 illustrates a third example of the circuit configuration of the conventional digital noise generator.

The configuration of this digital noise generator is such that a PAM/PCM converter 30 is added to the configuration shown in Fig. 3.

In other words, the pseudo-random noise signal outputted from an adder 27 is a pulse amplitude-modulated signal, i.e., a PAM signal. In cases where a PCM noise signal is required in DSI equipment or the like, it is necessary to generate a PCM pseudo-random noise signal by converting the

PAM signal to a PCM signal. The PAM/PCM converter 30 performs this PAM/PCM conversion.

The digital noise generators provided with the above-described configurations have the following problems:

1) A large-scale circuit configuration is necessary for securing the randomness of the pseudo-random noise signal.

In other words, the greater the number of bits of a shift register subject to addition by the adder, the greater the randomness of the pseudo-random noise signal.

Accordingly, in order to enhance the randomness of the pseudo-random noise signal, it is significant to increase the number of bits of the shift register. However, an increase in the number of bits of the shift register leads to greater numbers of AND circuits and scale factor circuits both corresponding to the respective bits. These are a factor enlarging the circuit configuration.

Meanwhile, if the weighting by the use of the scale factor circuits is effected with a greater weight, it is possible to enhance the randomness of the pseudo-random noise signal without resulting in an increased number of bits of the shift register. In this case, however, the code length becomes longer in correspondence with the degree of weighting, so that the configuration of the adder becomes complicated.

2) In order to generate the pseudo-random noise signal of PCM, a PAM/PCM converter is necessary, so that the circuit configuration becomes complicated.

Accordingly, an object of the present invention is to realize a pseudo-random noise signal having a sufficient amplitude characteristic and randomness through a simpler circuit configuration, thereby overcoming the above-described drawbacks of the conventional art.

To this end, a digital noise generator in accordance with the present invention comprises:

1) a pseudo-random bit sequence generator for generating and outputting a pseudo-random bit sequence;

2) an amplitude control circuit for converting an amplitude control signal supplied from an external circuit to an amplitude signal in accordance with a predetermined conversion rule; and

3) a PCM code-generating shift register which fetches the pseudo-random bit sequence and the amplitude signal and generates and outputs a pseudo-random noise signal which is a PCM code.

A description will be given hereinunder of the operation of the digital noise generator having the above-described configuration. First, a pseudo-random bit

sequence is generated by the pseudo-random bit sequence generator. Meanwhile, an amplitude control signal is converted to an amplitude signal. This conversion is effected on the basis of a predetermined conversion rule.

Furthermore, the pseudo-random bit sequence and the amplitude signal are fetched by the PCM code-generating shift register and are outputted as a pseudo-random noise signal which is a PCM code.

Generally, the randomness of a pseudo-random noise signal in PCM means uniformity in the signal strength of a pseudo-random noise signal. Since the pseudo-random noise signal has a discrete spectrum, the randomness is determined by a pitch Δf of a frequency spectrum and the amplitude of the frequency spectrum.

For instance, in a spectrum distribution shown in Fig. 5, the state in which the pitch Δf of a frequency spectrum of the pseudo-random noise signal is sufficiently small and the amplitude is substantially fixed is referred to as a state of good randomness.

The pitch Δf of the frequency spectrum is determined by the following formula in correspondence with a number of samples Nmax and a sampling period T:

$$\Delta f = 1/(Nmax \times T)$$

where Nmax is the length of the pseudo-random bit sequence.

Accordingly, if the number of samples Nmax is sufficiently large, the pitch Δf of the frequency spectrum of the pseudo-random noise signal becomes small, and an amplitude-frequency characteristic which is closer to white noise is obtained.

Meanwhile, the amplitude of a pseudo-random noise signal is determined by an amplitude code-word which is an output of the amplitude control circuit. That is, the amplitude control signal determines the amplitude of the pseudo-random noise signal outputted from the PCM code-generating shift register.

Accordingly, the conventional AND circuits, scale factor circuits, adder circuit, and PAM/PCM converter can be dispensed with, and the randomness and a good amplitude characteristic can be realized with a simple configuration.

As a means for converting the amplitude control signal to the amplitude code-word, there is a means in which a nonvolatile memory is incorporated in the amplitude control circuit, and a code conversion table is stored in the nonvolatile memory so as to refer to the code conversion table.

The code conversion table is prepared in advance in accordance with a predetermined conversion rule. As the conversion rule, it suffices to adopt, for instance, a

conversion rule based on the μ-law PCM coding rule or the A-law PCM coding rule that is stipulated in the CCITT recommendation G.711, or a conversion rule based on a linear PCM coding rule.

The PCM code-word-generating shift register operates in response to a PCM sampling clock signal of a predetermined period and a serial clock for outputting a PCM code-word, both supplied from an external circuit.

The PCM sampling clock signal is supplied to the pseudo-random bit sequence generator and the PCM code-word-generating shift register. An output timing of the pseudo-random bit sequence generator and an input timing of the PCM code-word-generating shift register are synchronized with each other by means of the PCM sampling clock signal.

The serial clock for outputting a PCM code-word is a clock for imparting a serial output timing of a pseudo-random noise signal from the PCM code-word-generating shift register.

In addition, the pseudo-random bit sequence generated by the pseudo-random bit sequence generator and the amplitude code-word generated by the amplitude control circuit are stored in the PCM code-word-generating shift register. For instance, the pseudo-random bit sequence is stored in the most significant bit of the PCM code-word-

generating shift register, and the amplitude code-word in the remaining bits.

In other words, if the number of bits of the PCM code-word-generating shift register is set to 8, the pseudo-random bit sequence is stored in the 0th bit, and the amplitude code-word in the 1st to 7th bits.

In a PCM coding rule, the 0th bit generally indicates the polarity. Accordingly, the amplitude of the pseudo-random noise signal is determined by the 1st to 7th bits of the PCM code-word-generating shift register.

As described above, in accordance with the present invention, it is possible to control the amplitude of the pseudo-random noise signal without depending on the configuration of the pseudo-random bit sequence generator. In addition, in accordance with the present invention, it is possible to secure a necessary degree of randomness for the pseudo-random noise signal. Furthermore, the pseudo-random noise signal outputted from the PCM code-word-generating shift register conforms to the PCM coding rule, and the configuration of PAM/PCM converter becomes unnecessary. Moreover, since the code conversion table for signal conversion in the amplitude control circuit can be calibrated in correspondence with a PCM coding rule, the digital noise generator in accordance with the present invention can be adapted to various PCM coding rules.

The invention is described further hereinafter, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram illustrating a digital noise generator in accordance with an embodiment of the present invention;

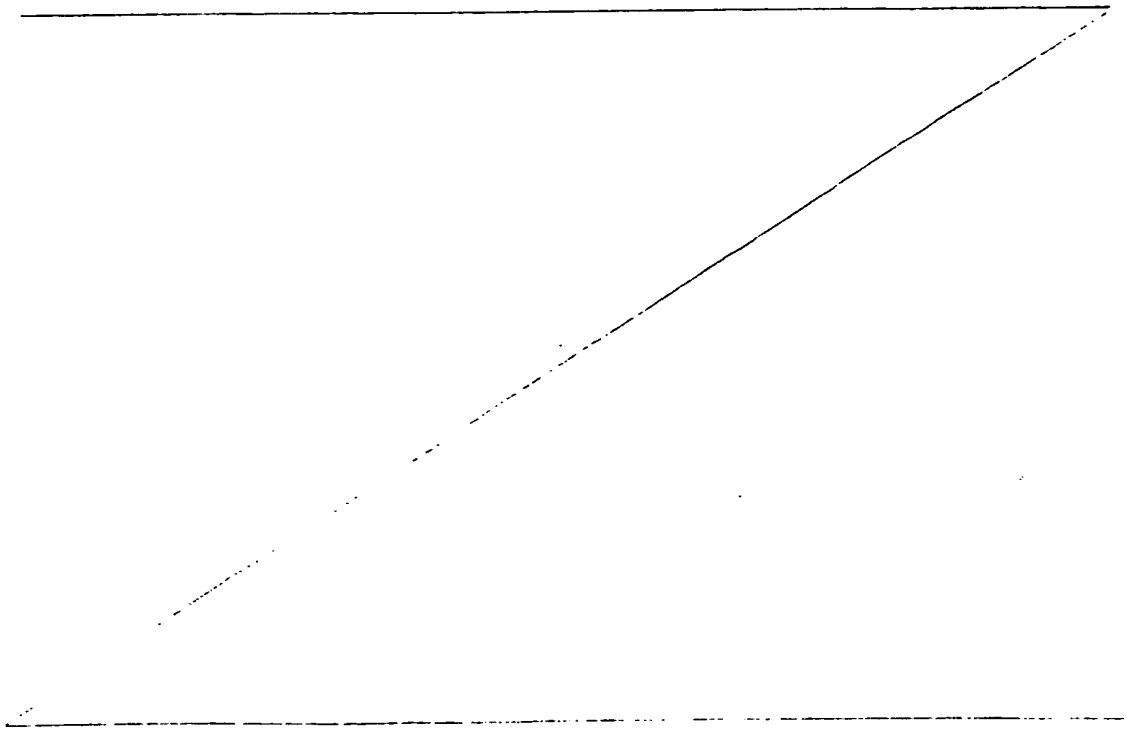
Fig. 2 is a circuit diagram illustrating a configuration of a digital noise generator in accordance with a first prior art;

Fig. 3 is a circuit diagram illustrating a configuration of a digital noise generator in accordance with a second prior art;

Fig. 4 is a circuit diagram illustrating a configuration of a digital noise generator in accordance with a third prior art; and

Fig. 5 is a diagram illustrating an amplitude-frequency characteristic of a pseudo-random noise signal.

Fig. 1 illustrates a configuration of a digital noise generator in accordance with an embodiment of the present invention.



The digital noise generator comprises a pseudo-random bit sequence generator 43 including an exclusive-OR circuit 41 and a shift register 42; an amplitude control circuit 51; and a PCM code-word-generating shift register 52.

The pseudo-random bit sequence generator 43 and the amplitude control circuit 51 are connected to the PCM code-word-generating shift register 52.

A description will be given hereinunder of the operation of this embodiment.

An output and intermediate output of the shift register 42 are subjected to an exclusive-OR operation by the exclusive-OR circuit 41 in the same way as the above-described conventional art. A signal obtained as a result of this operation is fed back to the shift register 42. As this operation is repeated with respect to the respective bits of the shift register 42, the output of the shift register 42 constitutes a so-called pseudo-random bit sequence.

Meanwhile, an amplitude control signal supplied from an external circuit is converted to an amplitude code-word on the basis of a code conversion table stored in a nonvolatile memory incorporated in the amplitude control circuit 51.

In this embodiment, the code conversion table is based on the μ-law PCM coding rule stipulated in the International

Telegraph and Telephone Consultative Committee (CCITT) recommendation G.711.

The pseudo-random bit sequence and the amplitude code-word are stored in each bit of the PCM code-word-generating shift register 52.

In this embodiment, the number of bits of the PCM code-word-generating shift register 52 is 8, and the pseudo-random bit sequence is fetched to the most significant 0th bit and the amplitude code-word to the 1st to 7th bits. The transmission and receipt of the pseudo-random bit sequence are effected in response to a PCM sampling clock signal of a predetermined period supplied from an external circuit.

In the μ-law PCM coding rule stipulated in the CCITT recommendation G.711, the most significant bit is a polarity bit indicating a polarity. If the polarity bit is "1", the sample value is positive, and if it is "0", the sample value is negative.

In this coding rule, the lower bits (in this embodiment, the lower seven bits) indicate the amplitude of a sample value. For instance, if the lower seven bits are "0000000", it indicates the maximum amplitude, while if it is "1111111", it indicates the minimum amplitude. Furthermore, the amplitude characteristic is a polygonal line characteristic composed of eight segments each for the

positive and the negative, and this characteristic approximates a logarithmic characteristic.

Each time sampling is effected, data must be fed to the most significant bit of the PCM code-word-generating shift register 52, i.e., the polarity bit. To realize this, the PCM sampling clock is also supplied to the pseudo-random bit sequence generator 43 in the same way as described above.

The PCM code-word-generating shift register 52 generates a pseudo-random random noise signal which conforms to the PCM coding rule, on the basis of the pseudo-random bit sequence and the amplitude code-word thus stored.

In this embodiment, if an m-series pseudo-random bit sequence is to be generated using an n-bit shift register as the shift register 42, the length of the bit sequence, Nmax, becomes $2^n - 1$. If it is assumed that the period T of the PCM sampling clock signal is 125 μsec, the pitch Δf of a frequency spectrum can be expressed by the following formula:

$$\Delta f = 8/(2^n - 1) \quad \text{(kHz)}$$

Furthermore, the PCM code-word-generating shift register 52 outputs a pseudo-random noise signal in response to a serial clock signal for outputting a PCM code-word which is supplied from an external circuit.

Accordingly, the pseudo-random noise signal which conforms to the PCM coding rule is supplied to, for instance, the DSIE as white noise.

It should be noted that the PCM coding rule in the present invention is not restricted to the μ-law PCM coding rule stipulated in the CCITT recommendation G.711. For instance, it is possible to adopt the A-law PCM coding rule stipulated in said recommendation G.711. Furthermore, a linear coding rule may also be adopted. It suffices if the code conversion table is calibrated in correspondence with a coding rule adopted.

CLAIMS

1. A digital noise generator comprising a pseudo-random bit sequence generator for generating and outputting a pseudo-random bit sequence, an amplitude control circuit for converting an amplitude control signal to an amplitude code-word in accordance with a predetermined conversion rule and a PCM code-word-generating shift register which fetches the pseudo-random bit sequence and the amplitude code-word and generates and outputs a pseudo-random noise signal which conforms to a PCM coding rule.

2. A digital noise generator as claimed in claim 1, wherein the amplitude control circuit comprises a nonvolatile memory for storing a code conversion table based on a rule of conversion from the amplitude control signal to the amplitude code-word, the amplitude control signal being converted to the amplitude code-word by reference to the code conversation table.

3. A digital noise generator as claimed in claim 2, wherein the nonvolatile memory stores the code conversion table for converting the amplitude control signal to the PCM code-word based on the μ-law PCM coding rule stipulated in the CCITT recommendation G.711.

4. A digital noise generator as claimed in claim 2, wherein the nonvolatile memory stores the code conversion table for converting the amplitude control signal to the PCM code-word based on the A-law PCM coding rule stipulated in the CCITT recommendation G.711.

5. A digital noise generator as claimed in claim

2, wherein the nonvolatile memory stores the code conversion table for converting the amplitude control signal to the PCM code-word based on a linear PCM coding rule.

6. A digital noise generator as claimed in any of claims 1 to 5, wherein the amplitude control circuit outputs the pseudo-random bit sequence in response to a PCM sampling clock signal of a predetermined period which is supplied from an external circuit, the PCM code-word-generating shift register being adapted to fetch the pseudo-random bit sequence and the amplitude code-word in response to the PCM sampling clock signal.

7. A digital noise generator as claimed in any preceding claim, wherein the pseudo-random bit sequence is stored in the most significant bit of said PCM code-word generating shift register and the amplitude code-word is stored in the remaining bits.

8. A digital noise generator as claimed in any preceding claim, wherein the PCM code-word-generating shift register serially outputs the pseudo-random noise signal in response to the serial clock signal for outputting a PCM code-word.

9. A digital noise generator as claimed in any preceding claim, wherein the PCM code-word-generating shift register comprises an 8-bit shift register.

10. A digital noise generator as claimed in any preceding claim, wherein the pseudo-random bit sequence generator includes a shift register with a predetermined number of bits and an exclusive-OR circuit for fetching an output and intermediate output of the shift register so as to determine an exclusive-OR and effect a feedback input to the shift register and which is adapted to output an output of the shift register as a pseudo-random bit sequence.

11. A digital noise generator as hereinbefore

described with reference to and as illustrated in Fig. 1 and Fig. 5 of the accompanying drawings.

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